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L7	1418	hot adj2 insert$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L13	18	L11 and L12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L16	3493	L14 and L15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L18	5	L16 and L17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L24	1418	hot adj2 insert$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L25	15176	size adj2 information	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L26	19198	memory adj2 size	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L31	5	L28 and L29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L32	1	L31 and L30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L33	6622	memory adj2 allocation	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L34	351	expandable adj2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
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L36	18	L33 and L34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L37	0	L36 and L31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:43
L38	127	(Murayama near Hideki).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:44
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L42	535	(Ishii near Yasuhiro).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:44
L43	24	(Sasaki near Daisuke).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:44
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L45	0	L44 and L36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 13:44

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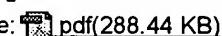
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Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1
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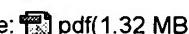
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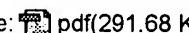
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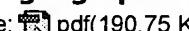
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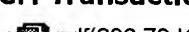
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Thomas Wollinger, Jorge Guajardo, Christof Paar
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July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3

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Cristiana Bolchini, Fabio Salice, Fabio A. Schreiber, Letizia Tanca
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António Muchaxo, Alexandre Sousa, Nuno Pereira, Helena Sarmento
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Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger
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Timothy Sherwood, Brad Calder
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Brad Eckert
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December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles**, Volume 29 Issue 5

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16 <u>Serverless network file systems</u>
Thomas E. Anderson, Michael D. Dahlin, Jeanna M. Neefe, David A. Patterson, Drew S. Roselli, Randolph Y. Wang
February 1996 **ACM Transactions on Computer Systems (TOCS)**, Volume 14 Issue 1

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Frank Vahid, Ann Gordon-Ross
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Wee Teck Ng, Peter M. Chen
August 1998 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 7 Issue 3
Full text available: pdf(123.18 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>index terms</u>

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Yervant Zorian, Sujit Dey, Michael J. Rodgers
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1 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques ▨
Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1
Full text available: 📄 pdf(288.44 KB)   Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

2 eNVy: a non-volatile, main memory storage system ▨
Michael Wu, Willy Zwaenepoel
November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29, 28 Issue 11, 5
Full text available: 📄 pdf(1.32 MB)   Additional Information: full citation, abstract, references, citings, index terms

This paper describes the architecture of eNVy, a large non-volatile main memory storage system built primarily with Flash memory. eNVy presents its storage space as a linear, memory mapped array rather than as an emulated disk in order to provide an efficient and easy to use software interface.Flash memories provide persistent storage with solid-state memory access times at a lower cost than other solid-state technologies. However, they have a number of drawbacks. Flash chips are ...

3 Services: ELF: an efficient log-structured flash file system for micro sensor nodes ▨
Hui Dai, Michael Neufeld, Richard Han
November 2004 **Proceedings of the 2nd international conference on Embedded networked sensor systems**

Full text available: pdf(291.68 KB)   Additional Information: full citation, abstract, references, index terms

An efficient and reliable file storage system is important to micro sensor nodes so that data can be logged for later asynchronous delivery across a multi-hop wireless sensor network. Designing and implementing such a file system for a sensor node faces various challenges. Sensor nodes are highly resource constrained in terms of limited runtime memory, limited persistent storage, and finite energy. Also, the flash storage medium on sensor nodes differs in a variety of ways from the traditiona ...

Keywords: eeprom, file system, flash, log structured, reliability, sensor

4 An efficient r-tree implementation over flash-memory storage systems
Chin-Hsien Wu, Li-Pin Chang, Tei-Wei Kuo
November 2003 **Proceedings of the 11th ACM international symposium on Advances in geographic information systems**
Full text available: pdf(190.75 KB)   Additional Information: full citation, abstract, references, index terms

For many applications with spatial data management such as Geographic Information Systems (GIS), block-oriented access over flash memory could introduce a significant number of node updates. Such node updates could result in a large number of out-place updates and garbage collection over flash memory and damage its reliability. In this paper, we propose a very different approach which could efficiently handle fine-grained updates due to R-tree index access of spatial data over flash memory. The ...

Keywords: GIS, R-tree, embedded systems, flash memory, spatial index structures, storage systems

5 Security on FPGAs: State-of-the-art implementations and attacks
Thomas Wollinger, Jorge Guajardo, Christof Paar
August 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 3
Full text available: pdf(296.79 KB)   Additional Information: full citation, abstract, references, index terms

In the last decade, it has become apparent that embedded systems are integral parts of our every day lives. The wireless nature of many embedded applications as well as their omnipresence has made the need for security and privacy preserving mechanisms particularly important. Thus, as field programmable gate arrays (FPGAs) become integral parts of embedded systems, it is imperative to consider their security as a whole. This contribution provides a state-of-the-art description of security issues ...

Keywords: Cryptography, FPGA, attacks, cryptographic applications, reconfigurable hardware, reverse engineering, security

6 Pen computing: a technology overview and a vision
André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3
Full text available: pdf(5.14 MB)   Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

7 Logical and physical design issues for smart card databases
Cristiana Bolchini, Fabio Salice, Fabio A. Schreiber, Letizia Tanca
July 2003 **ACM Transactions on Information Systems (TOIS)**, Volume 21 Issue 3

Full text available: pdf(1.12 MB)   Additional Information: full citation, abstract, references, citings, index terms

The design of very small databases for smart cards and for portable embedded systems is deeply constrained by the peculiar features of the physical medium. We propose a joint approach to the logical and physical database design phases and evaluate several data structures with respect to the performance, power consumption, and endurance parameters of read/program operations on the Flash-EEPROM storage medium.

Keywords: Design methodology, access methods, data structures, flash memory, personal information systems, smart card

8 How application/technology evolutions will shape classical EDA?: System-on-chip beyond the nanometer wall
Philippe Magarshack, Pierre G. Paulin
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(454.87 KB)   Additional Information: full citation, abstract, references, citings, index terms

In this paper, we analyze the emerging trends in the design of complex Systems-on-a-Chip for nanometer-scale semiconductor technologies and their impact on design automation requirements, from the perspective of a broad range SoC supplier. We present our vision of some of the key changes that will emerge in the next five years. This vision is characterized by two major paradigm changes. The first is that SoC design will become divided into four mostly non-overlapping distinct abstraction levels. ...

Keywords: design automation tools, embedded software technologies, multi-processor systems, network-on-chip, reconfigurable systems, system-on-chip

9 Papers: Wireless data communications using DECT air interface
António Muchaxo, Alexandre Sousa, Nuno Pereira, Helena Sarmento
April 1999 **ACM SIGCOMM Computer Communication Review**, Volume 29 Issue 2

Full text available: pdf(1.25 MB)   Additional Information: full citation, abstract, references, citings

DECT is an approved ETSI standard for cordless communications, defined as a general radio access technology that can be used as the air interface to any network. In addition to the well-established voice service, it supports data communications. DECT currently addresses low bit rates, but additional modulation options have recently been included for high-speed, up to 2Mbps. In this paper, we describe the hardware and software design of an entire wireless communications system to be used in SOHO ...

10 Session summaries from the 17th symposium on operating systems principle (SOSP'99)
Jay Lepreau, Eric Eide
April 2000 **ACM SIGOPS Operating Systems Review**, Volume 34 Issue 2

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11 Designing computer systems with MEMS-based storage
Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger

November 2000 **Proceedings of the ninth international conference on Architectural support for programming languages and operating systems**, Volume 34 , 28 Issue 5 , 5

Full text available: pdf(439.06 KB) Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4-74X over ...

12 <u>Designing computer systems with MEMS-based storage</u>

Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger

November 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 11

Full text available: pdf(439.06 KB) Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

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13 <u>Caches and Memory Systems: Patchable instruction ROM architecture</u>

Timothy Sherwood, Brad Calder

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Full text available: pdf(299.03 KB) Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Increased systems level integration has meant the movement of many traditionally off chip components onto a single chip including a processor, instruction storage, data path, and local memory. The design of these systems is driven by two conflicting goals, the need for reduced area and the need for rapid development times. The two current design options for instruction storage, ROM and Flash, are each highly optimized to one of these two goals but provide little compromise between them. ROM is u ...

14 <u>Firmware factory & forth</u>

Brad Eckert

December 1999 **ACM SIGPLAN Notices**, Volume 34 Issue 12

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15 <u>Serverless network file systems</u>

T. E. Anderson, M. D. Dahlin, J. M. Neefe, D. A. Patterson, D. S. Roselli, R. Y. Wang

December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles**, Volume 29 Issue 5

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16 <u>Serverless network file systems</u>

Thomas E. Anderson, Michael D. Dahlin, Jeanna M. Neefe, David A. Patterson, Drew S. Roselli, Randolph Y. Wang

February 1996 **ACM Transactions on Computer Systems (TOCS)**, Volume 14 Issue 1

Full text available: pdf(2.69 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

We propose a new paradigm for network file system design: serverless network file systems. While traditional network file systems rely on a central server machine, a serverless system utilizes workstations cooperating as peers to provide all file system services. Any machine in the system can store, cache, or control any block of data. Our approach uses this location independence, in combination with fast local area networks, to provide better performance and scalability th ...

Keywords: RAID, log cleaning, log structured, log-based striping, logging, redundant data storage, scalable performance

17 <u>A self-optimizing embedded microprocessor using a loop table for low power</u>

Frank Vahid, Ann Gordon-Ross
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(230.48 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

Keywords: cores, embedded systems, low-power, parameterized architectures, platforms, self-optimizing architecture, system-on-a-chip, tuning

18 <u>The Chinook hardware/software co-synthesis system</u>

Pai H. Chou, Ross B. Ortega, Gaetano Borriello
September 1995 **Proceedings of the 8th international symposium on System synthesis**

Full text available: pdf(79.55 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>
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Abstract: Designers of embedded systems are facing ever tighter constraints on design time, but computer-aided design tools for embedded systems have not kept pace with these trends. The Chinook co-synthesis system addresses the automation of the most time-consuming and error-prone tasks in embedded controller design, namely the synthesis of interface hardware and software needed to integrate system components, the migration of functions between processors or custom logic, and the co-simulation ...

Keywords: Chinook hardware/software co-synthesis system, computer-aided design tools, custom logic, design co-simulation, design time constraints, embedded controller design, error-prone tasks, function migration, interface hardware, interface software, logic CAD, logic design, microcontrollers, microprocessors, real-time systems, software tools, system components integration

19 <u>Integrating reliable memory in databases</u>

Wee Teck Ng, Peter M. Chen
August 1998 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 7 Issue 3

Full text available: pdf(123.18 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>index terms</u>

Recent results in the Rio project at the University of Michigan show that it is possible to create an area of main memory that is as safe as disk from operating system crashes. This paper explores how to integrate the reliable memory provided by the Rio file cache into a database system. Prior studies have analyzed the performance benefits of reliable memory;

we focus instead on how different designs affect reliability. We propose three designs for integrating reliable memory into databases: non ...

Keywords: Main memory database system (MMDB), Recovery, Reliability

20 <u>Session 8D: embedded tutorial: Test of future system-on-chips</u>
Yervant Zorian, Sujit Dey, Michael J. Rodgers
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: <u>pdf(140.88 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SOCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of multimillion transistor chips. However, to mak ...

Results 1 - 20 of 200   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> <u>8</u> <u>9</u> <u>10</u>   <u>next</u>